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09/548,849	04/13/2000	Kent Vuong	PA1084US	7221

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EXAMINER	
TRAN, CON P	

ART UNIT	PAPER NUMBER
2644	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/548,849	Applicant(s) VUONG ET AL.	
	Examiner Con P. Tran	Art Unit 2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-18* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. **Claims 1-2** are rejected under 35 U.S.C. 102(e) as being anticipated by Rao et al. U.S. Patent 6,253,293 (hereinafter, "Rao").

Regarding **claim 1**, Rao teaches a method for processing audio information in a multiple processor audio decoder (100 having first DSPA 200a; see Fig. 2, 3, and respective portions of the specification), comprising the steps of:

providing an apparatus (a DSPB 200b , Fig. 2; see col. 5, lines 7-34) having a plurality of elements running in parallel with the DSP (the DSPA 200a can work in parallel with DSPA 200a; col. 9, line 51 – col. 10, line 11);

configuring the apparatus to perform a function according to a configuration setup (see Figs. 1C, 3; col. 4, line 59 – col. 5, line 6); and

employing the apparatus for accessing data from the elements in a pipeline structure to maximize utilization of the elements (col. 9, line 51 – col. 10, line 11).

Regarding **claim 2**, Rao teaches the method of claim 1 wherein the function is usable in audio algorithms (col. 9, line 55 – col. 10, line 11).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 3-5, and 7-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al. U.S. Patent 6,253,293 (hereinafter, "Rao") in view of Huang U.S. Patent 6,430,529, and further in view of Prakash U.S. Patent 6,405,227.

Regarding **claim 3,** Rao teaches the method of claim 1. Rao further teaches wherein the function is selected from a group consisting of filtering (24-bit), double precision filtering (48-bit; filter bank; col. 6, lines 47-64), IFFT, IDCT (col. 10, lines 1-9). However, Rao does not explicitly disclose a method in which the processor function of pre-multiplication and post-multiplication. Huang discloses method of digital audio processing in which utilizing pre-multiplication and post-multiplication (col. 2, lines 29-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Huang teaching of pre-multiplication and post-multiplication with the method for processing of Rao for purpose of reducing the cost for practical implication, as suggested by Huang in column 2, lines 51-52.

However, Rao in view of Huang does not explicitly disclose method of filtering is biquad filtering, and double precision filtering is double precision biquad filtering.

Prakash discloses a digital filter chip in which filter G(z) of equalizer (512) using biquad filtering (Figs. 5, 7B; col. 10, lines 20-23), and double precision biquad filtering (filter 513, not shown in Fig. 6A, col. 6, lines 11-14; col. 9, lines 18-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Prakash teaching of biquad filtering, and double precision biquad filtering with the method for processing of Rao, Huang combination in order to simplifying calculation of coefficients, as suggested by Prakash in column 3, lines 18-20.

Regarding **claim 4**, Rao teaches the method of claim 1 wherein the plurality of elements includes: a first memory (203b) for storing data; a second memory (204) for storing data; a third memory for storing coefficient data (202b, Fig. 2; col. 5, lines 7-33).

However, Rao does not explicitly disclose a method in which: data storing in first memory is real part data; data storing in second memory is imaginary part data; a multiplier for processing the real part data, the imaginary part data, and the coefficient data; and an ALU for processing the real part data, the imaginary part data, and the coefficient data.

Huang discloses method in which utilizes complex-valued of pre-multiplication and post-multiplication, prepares and arranges the data samples (col. 2, lines 35-47), separates real and imaginary parts (col. 3, lines 53-56); and an post-multiplier (450) for processing the real part data, the imaginary part data, and the coefficient data (col. 8, lines 30-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Huang teaching of storing data with the method for processing data of Rao as claimed, for purpose of reducing the cost for practical implication, as suggested by Huang in column 2, lines 51-52.

Regarding **claim 5**, Huang further teaches wherein in a post-multiplication function, data is accessed in bit reverse order (to separate and shuffled final output sequence; (-1)^k; col. 8, lines 30-58).

Regarding **claim 7**, Rao in view of Huang teaches the method of claim 1. However, Rao does not explicitly disclose a method wherein performing a biquad function comprises the steps as claimed. Prakash discloses a method wherein performing a biquad function (24 bits, col. 9, lines 7-16; col. 10, lines 20-25) comprises the steps of:

receiving N + 1 samples of data x_n for n = m to n = m + N (input sample, col. 6, lines 11-14);

storing data including the samples of data in memory locations (data RAM 424, Fig. 4; col. 5, lines 29-32)

and calculating y_n according to the equation $y_n = b_0x_n + b_1x_{n-1} + b_2x_{n-2} + a_1y_{n-1} + a_2y_{n-2}$ (see col. 6 lines 11-26; col. 10, lines 20-31).

Rao in view of Prakash does not explicitly disclose a predefined order of memory locations to store data samples. It would be obvious to store samples of data in memory location in a predefined order in order to process the samples accordingly.

Regarding **claims 8-9,** Prakash further discloses biquad filter structure (600) in Figure 6A, data RAM (424, Fig. 4; col. 5, lines 29-32). It would be obvious to store samples of data in memory location of data RAM (424, Fig. 4; col. 5, lines 29-32) in a predefined order as claimed in order to process the samples accordingly. Furthermore, it would be obvious to increase index value of index numbers (m) and (K) for each loop (i) in order to calculate the output equation y_n efficiently.

Regarding **claim 10**, Rao in view of Huang teaches the method of claim 1. However, Rao does not explicitly disclose a method wherein performing a double precision biquad function comprises the steps as claimed. Prakash discloses a method wherein performing a double precision biquad function (48 bits, col. 9, lines 7-20) comprises the steps of:

receiving N + 1 samples of data x_n for n = m to n = m + N (input sample, col. 6, lines 11-14);

storing data including the samples of data in memory locations (data RAM 424, Fig. 4; col. 5, lines 29-32)

and calculating y_n according to the equation $y_n = b_0x_n + b_1x_{n-1} + b_2x_{n-2} + a_1yl_{n-1} + a_2yl_{n-2} + a_1yh_{n-1} + a_2yh_{n-2}$ (i.e., yl is equivalent to y; yh is equivalent to d; see col. 9, lines 20-37).

Rao in view of Prakash does not explicitly disclose a predefined order of memory locations to store data samples, and steps of calculating output. It would be obvious to store samples of data in memory location in a predefined order in order to process the samples accordingly.

Regarding **claims 11-12,** Prakash further discloses double precision biquad filter structure (650) in Figure 6B, data RAM (424, Fig. 4; col. 5, lines 29-32). It would be obvious to store samples of data in memory location of data RAM (424, Fig. 4; col. 5, lines 29-32) in a predefined order as claimed in order to process the samples

accordingly. Furthermore, it would be obvious to increase index value of index numbers (m) and (K) for each loop (i) in order to calculate the output equation y_n efficiently.

5. **Claims 13-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prakash U.S. Patent 6,405,227.

Regarding **claim 13**, Prakash discloses a method performing a biquad function (24 bits, col. 9, lines 7-16; col. 10, lines 20-25) comprises the steps of:

receiving N + 1 samples of data x_n for n = m to n = m + N (input sample, col. 6, lines 11-14);

storing data including the samples of data in memory locations (data RAM 424, Fig. 4; col. 5, lines 29-32)

and calculating y_n according to the equation $y_n = b_0x_n + b_1x_{n-1} + b_2x_{n-2} + a_1y_{n-1} + a_2y_{n-2}$ (see col. 6 lines 11-26; col. 10, lines 20-31).

Prakash does not explicitly disclose a predefined order of memory locations to store data samples. It would be obvious to store samples of data in memory location in a predefined order in order to process the samples accordingly.

Regarding **claims 14-15,** Prakash further discloses biquad filter structure (600) in Figure 6A, data RAM (424, Fig. 4; col. 5, lines 29-32). It would be obvious to store samples of data in memory location of data RAM (424, Fig. 4; col. 5, lines 29-32) in a predefined order as claimed in order to process the samples accordingly. Furthermore,

it would be obvious to increase index value of index numbers (m) and (K) for each loop (i) in order to calculate the output equation y_n efficiently.

Regarding **claim 16,** Prakash discloses a method performing a double precision biquad function (48 bits, col. 9, lines 7-20) comprises the steps of:

receiving N + 1 samples of data x_n for n = m to n = m + N (input sample, col. 6, lines 11-14);

storing data including the samples of data in memory locations (data RAM 424, Fig. 4; col. 5, lines 29-32)

and calculating y_n according to the equation $y_n = b_0x_n + b_1x_{n-1} + b_2x_{n-2} + a_1yl_{n-1} + a_2yl_{n-2} + a_1yh_{n-1} + a_2yh_{n-2}$ (i.e., yl is equivalent to y; yh is equivalent to d; see col. 9, lines 20-37).

Prakash does not explicitly disclose a predefined order of memory locations to store data samples, and steps of calculating output. It would be obvious to store samples of data in memory location in a predefined order in order to process the samples accordingly.

Regarding **claims 17-18,** Prakash further discloses double precision biquad filter structure (650) in Figure 6B, data RAM (424, Fig. 4; col. 5, lines 29-32). It would be obvious to store samples of data in memory location of data RAM (424, Fig. 4; col. 5, lines 29-32) in a predefined order as claimed in order to process the samples

accordingly. Furthermore, it would be obvious to increase index value of index numbers (m) and (K) for each loop (i) in order to calculate the output equation y_n efficiently.

Allowable Subject Matter

6. **Claim 6** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record disclosed method for processing audio information in pipeline structure, but failed to disclose or fairly suggested wherein data is accessed in a four-cycle pipeline structure in a pre-multiplication function, in an IFFT function, and in a post-multiplication function, data is accessed in a six-cycle pipeline structure in a biquad mode, and data is accessed in a nine-cycle pipeline structure in a double precision biquad mode.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inventor	Publication	Number	Disclosure
Matsuo et al.	US Patent	5,901,301	A data processor for high-speed digital

			signal processing and a method of processing data for high-speed digital signal processing.
Mills	US Patent	6,311,204	A method and apparatus for preventing interference between simultaneously-running processes in a set top box processing system which attempt to access certain shared processing hardware such as a drawing acceleration engine.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Con P. Tran, whose telephone number is (703) 305-2341. The examiner can normally be reached on M - F (8:30 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office at telephone number (703) 306-0377.

cpt CPJ
May 17, 2004

XU MEI
PRIMARY EXAMINER